

# United States Patent and Trademark Office

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/532,216	08/31/2005	Yutaka Ozaki	26738U	6735
<sup>20529</sup> NATH & ASSO	7590 01/14/2008 CIATES		EXAMINER	
112 South Wes	Street		PHILOGENE, HAISSA	
Alexandria, VA 22314			ART UNIT	PAPER NUMBER
			2821	
			MAIL DATE	DELIVERY MODE
			01/14/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

•	Application No.	Applicant(s)			
	10/532,216	OZAKI, YUTAKA			
Office Action Summary	Examiner	Art Unit			
	Haissa Philogene	2821			
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply					
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).					
Status					
<ol> <li>Responsive to communication(s) filed on 10 October 2007.</li> <li>This action is FINAL. 2b)  This action is non-final.</li> <li>Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.</li> </ol>					
Disposition of Claims					
4) Claim(s) 1-12 is/are pending in the application. 4a) Of the above claim(s) is/are withdraw 5) Claim(s) is/are allowed. 6) Claim(s) 1-3,7 and 8 is/are rejected. 7) Claim(s) 4-6 and 9-12 is/are objected to. 8) Claim(s) are subject to restriction and/or Application Papers  9) The specification is objected to by the Examiner 10) The drawing(s) filed on 22 April 2005 is/are: a) Applicant may not request that any objection to the of Replacement drawing sheet(s) including the correction.	vn from consideration.  relection requirement.  r.  ☑ accepted or b) ☐ objected to be drawing(s) be held in abeyance. See	e 37 CFR 1.85(a).			
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.					
Priority under 35 U.S.C. § 119					
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  a) All b) Some * c) None of:  1. Certified copies of the priority documents have been received.  2. Certified copies of the priority documents have been received in Application No  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  * See the attached detailed Office action for a list of the certified copies not received.					
Attachment(s)  1) Notice of References Cited (PTO-892)  2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  3) Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 8/24/07.	4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal Pa	ite			

#### **DETAILED ACTION**

## Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi et al, Pub. No. 2003-0001848 in view of Yoneda et al., Pub. No. 2003-058125, both cited by Applicant.

As per claim 1, Choi discloses in Fig. 7 a LED driving device comprising: a power supply voltage generator (1) and an applied voltage former (20) that converts a voltage generated in the power supply voltage generator into the applied voltage value to apply to the LED (3). Choi does not disclose an applied voltage storage that stores therein an applied voltage value on an each-color basis corresponding to a minimum emission voltage of an LED of each of colors, red, green and blue, provided in a display device and said applied voltage value to apply to the LED of each of colors. Yoneda discloses in Figs. 1, 5, 6 and 15 a LED driving device having a data storage means (EEPROM) in CPU (110), said data capable of being applied voltage V or drive current value, thereby readable as an applied voltage storage that stores therein an applied voltage value on an each-color basis corresponding to a minimum emission voltage of an LED of each of colors, red, green and blue, on the basis of a predetermined lighting property, provided in a display device (150) and said applied voltage value to apply to the LED of each of colors via driving means (154f). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to employ the applied voltage storage as taught by Yoneda into the Choi's LED driving device, because it would allow a reproduction of a desired color of an image at a low cost even though LEDs are used as a light source such as back light or front light.

As per claims 2, 3 and 7, Choi in view of Yoneda discloses the claimed invention substantially as explained above. In addition, Yoneda discloses the values being the same on the same color, while being different between different colors (when using the formula of drawing 11 and see also paragraph [0048] in translated version); wherein the applied voltage storage (EEPROM in CPU (110)) stores independent applied voltage values for LEDs of the same color via independent driving means 154f as shown in Figs. 5 and 6; wherein among LEDs ( 254 of Fig.15) of red, green and blue, red LEDs are capable of undergoing cascade connection since the red LEDs have spectral characteristic that differs from that of blue or green LEDs with minimum value lower than that of blue or green LEDs (see paragraph [0048] of the translated version).

As per claim 8, Choi in view of Yoneda discloses the claimed invention substantially as explained above. Further, Yoneda discloses in Fig.6 that a power supply voltage generator generates a single voltage value (V), and an applied voltage former or driving means (154f) has a D/A converter (DAC) that performs digital/analog conversion on a voltage value as data stored in the applied voltage storage (EEPROM in CPU (110), and a voltage varying section (formed by the remaining components in the driving means) that converts the single voltage generated in the power supply voltage generator (V) via the controlled booster circuit part into a voltage corresponding to an analog value converted in the D/A converter (DAC).

### Allowable Subject Matter

Claims 4-6 and 9-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

#### Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Haissa Philogene whose telephone number is (571) 272-1827. The examiner can normally be reached on 8:30 A.M.-6:00 P.M..

Art Unit: 2821

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Douglas W. Owens can be reached on (571)272-1662. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

hp

Haissa Philogona Primary Argminer